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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,198	07/20/2005	Leon Maria Albertus Van De Logt	NL 020601	2711

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
ISLA RODAS, RICHARD	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/520,198	VAN DE LOGT ET AL.	
	Examiner	Art Unit	
	Richard Isla-Rodas	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-8* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/04/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: The specification is missing a clear description of the interconnects as described in page 1, line 3.

Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show interconnects as described in claim 1. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. Claims 1, 4-8 is rejected under 35 U.S.C. 102(e) as being anticipated by the US Patent to De Jong et al. (6,622,108).

In terms of claim 1, De Jong et al. show in Figures 4 and 6, an electronic circuit (402) comprising a plurality of input/output (I/O) nodes (nodes for i1, i2, i3, o1, o2) for connecting the electronic circuit to a further electronic circuit (210) via interconnects (408, 412 and 410), a test unit (406) comprising a combinatorial circuit (602) having a plurality of inputs (i1, i2, i3) and an output (o1), the combinatorial circuit implementing an exclusive logic function, the I/O nodes being logically connected (See column 1, lines 22-25) to the test unit in the test mode, wherein a first selection of the I/O nodes (nodes for i1, i2, i3) is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit (602), and a second selection of the I/O node (o1, o2) comprising a first I/O node (o1) and is arranged to carry respective output signals, the first I/O node (o1) coupled to the output of the combinatorial circuit (602), characterized in that the second selection of the I/O nodes (o1,o2) further comprises a second I/O node (o2) that is coupled to an I/O node (i3) from the first selection of the I/O nodes (i1, i2, i3) in the test mode via a connection (604) that bypasses the combinatorial circuit (602).

As to claim 4, De Jong et al. teach that an alternative is to provide the test circuit with a dedicated test control node, in addition to the I/O nodes, to control whether the circuit is to behave in the normal operational mode or in the test mode (See column 8, lines 35-38).

As to claim 5, De Jong et al. show in Figure 4, a main unit (404) which is logically connected to the I/O nodes (See column 1, lines 22-25), in a functional mode of the electronic circuit, the main unit being arranged to bring the electronic circuit into the test mode upon receipt of a test control signal in a form of a predefined bit pattern through at least a subset of the first selection of I/O nodes (See column 9, lines 61-67).

As to claim 6, in addition to that stated with regards to claim 4, De Jong et al. show in Figure 4, an electronic circuit (402) as claimed in claim 4 and a further electronic circuit (210), the electronic circuit having interconnects (410, 412, 408) with the further electronic circuit, characterized in that the further electronic circuit (210) is arranged to provide the electronic circuit with the test control signal (408) and to provide the first selection of I/O nodes with test patterns for testing the interconnects (See column 9, lines 64-65).

As to claim 7, in addition to that stated with regards to claim 6, De Jong et al. show in Figure 4, the further electronic circuit (210) is arranged to receive test result data (through 1:m) from the second selection of I/O nodes.

As to claim 8, De Jong et al. teach through Figures 4 and 6, an method for testing interconnects between an electronic circuit and a further electronic circuit (210), the electronic circuit (402) comprising a plurality of input/output (I/O) nodes (nodes for i1, i2, i3) for connecting the electronic circuit to the further electronic circuit (210) via interconnects (408, 412 and 410), a test unit (406) comprising a combinatorial circuit (602) having a plurality of inputs (nodes for i1, i2, i3) and an output (o1), the combinatorial circuit implementing an exclusive logic function, the I/O nodes being

logically connected (See column 1, lines 22-25) to the test unit in the test mode, wherein a first selection of the I/O nodes (nodes for i1, i2, i3) is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit (602), and a second selection of the I/O node (o1, o2) comprising a first I/O node (o1) and is arranged to carry respective output signals, the first I/O node (o1) coupled to the output of the combinatorial circuit (602), characterized in that the second selection of the I/O nodes (o1,o2) further comprises a second I/O node (o2) that is coupled to an I/O node (i3) from the first selection of the I/O nodes in the test mode via a connection (604) that bypasses the combinatorial circuit (602) and the method further comprising the step of logically connecting the test unit to the interconnects (See column 1, lines 22-25), putting test data on the interconnects by the further electronic circuit (See column 9, lines 64-65), and receiving test result data (using lines 1:m) through the first I/O node (nodes for i1, i2, i3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to De Jong et al. (6,622,108) in view of the US Patent to Chou (6,591,384).

In terms of claim 2, De Jong et al. teach all the claimed elements as disclosed above, except for the second selection of I/O nodes further comprising a third I/O node being coupled to a further I/O node from the first selection of I/O nodes in the test mode via a further connection that bypasses the combinatorial circuit. Chou, drawn to circuits for parallel testing of DRAM devices, teaches in Figure 3 and 4B, an electronic circuit (100A), connected to a test unit (340A), the test unit comprising a combinatorial circuit (306, 308) implementing an exclusive logic function, a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit (A'B'C'D'), and a second selection of I/O nodes (IO_0, IO_1, IO_2), comprising a first I/O node (IO_0) arranged to carry respective output signals, the first I/O node (IO_0) being coupled to the output of the combinatorial circuit. The circuit is characterized in that the second selection of the I/O nodes further comprises a second I/O node (IO_1) that is coupled to an I/O node from the first selection of the I/O nodes via a connection (102A) that bypasses the combinatorial circuit. The second selection of I/O nodes (IO_0, IO_1, IO_2), further comprises a third I/O node (IO_2) being coupled to a further

I/O node from the first selection of I/O nodes via a further connection (102A) that bypasses the combinatorial circuit. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the teaching of a second node bypassing a combinatorial circuit as taught by Chou, to include a second node bypassing the combinatorial circuit in De Jong et al. device, in order to allow an additional bit for comparing to the output of the combinatorial circuit and thus increasing accuracy in the testing process.

Allowable Subject Matter

7. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. In terms of claim 3, no prior art was found that contained the limitations of the base claim in addition to having the second I/O node coupled to a buffer and the third I/O node coupled to an inverter.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents to Mc Donnell et al. (5,241,265), Hirooka et al. (6,144,595), Hidaka et al. (6,400,621), Russell (4,556,840) and Mattes (5,224,107).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571) 272-5056. The examiner can normally be reached Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ~~Nestor Ramirez~~ Wael Fahmy can be reached on (571) 272-~~2034~~ 1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard Isla-Rodas

12/24/05
PARESH PATEL
PRIMARY EXAMINER